MANIPAL UNIVERSITY JAIPUR

International Winter School-Manipal University Jaipur [IWSMUJ]-2023

[Hybrid Mode]

Course/Project Overview

Name of Course/Project- Design and analysis of FeFET for Memory Device Application

Name of instructor: 1. Dr. Kulwant Singh, Assoc. Professor, ECE
2. Dr. Dhaneshwar Mishra, Assoc. Professor (Senior Scale), Mech. Eng.
3. Dr. Nandakishor Yadav, Center Nanoelectronic Technologies CNT, Fraunhofer Institute for Photonic Microsystems IPMS, Germany

Session: Jan.-Feb. 2023
Language of instruction: English
Number of contact hours: 36
Credit awarded: 03

Objective of Course/Project

- To carry out a design and simulation study on ferroelectric thin film optimization
- To carry out device structure optimization of **FeFET**
- To propose a solution to improve endurance without a retention penalty

Syllabus: Preliminary knowledge about MOSFET Technology

Organization of Project

Total contact hrs 36		
1st week:	10 hrs (classes)	2 hrs (self-study/project)
2nd week:	10 hrs (classes)	2 hrs (Mid-term assessment/discussion)
3rd week:	10 hrs (classes)	2 hrs
4th week:	6 hrs (Classes)	2hrs (End term assesment)

Mode of lectures: Hybrid mode lecture/videos/case study/ discussion/ workshop/

Brief profile of the instructor

Dr. Kulwant Singh is currently Assoc. professor at Department of Electronics and Communication Engineering, and Deputy Director at E-Cell, Manipal University Jaipur. He has completed his Ph.D. in VLSI Technology from NIT Calicut, Kerala, India in 2015. His major area of expertise are Semiconductor Device Technology, MEMS Sensors, Biosensors, Energy Storage Devices, etc. Dr. Singh has more than 8 years R&D experience in a semiconductor cleanroom environment for leading-edge semiconductor/MEMS device technology work (wafer cleaning, Thermal oxidation, thin film deposition using PVD/CVD techniques, ion implantation, diffusion process, lithography, dry & wet etching, bulk-micromachining optimization, wafer-level testing, and device packaging). He is involved in teaching learning at University/technical institutions level since more than 12 years. He has strong understanding of VLSI/MEMS device design, fabrication process, and various thin film analysis techniques – AFM, XRD, SEM, EDS, thin-film thickness measurements. He has proven ability to collaborate with local and overseas teams on projects and good project management skills. Dr. Singh has published many peers reviewed international journal articles of more than 90 impact factor, and two patents are published and some are in the process.

Dr. Dhaneshwar Mishra is currently Assoc. Professor (Senior Scale) at Department of Mechanical Engineering, Manipal University Jaipur. He has completed PhD. in Mechanical engineering from Ajou University Suwon, South Korea in 2011. His domain of research is structural mechanics, defect/fracture mechanics, solid mechanics, computational material science, etc. He has published 19 SCI journal articles, 3 book chapters, and 12 conference proceedings, and presented in 23 international conferences worldwide. Dr. Mishra completed Masters of Engineering with specialization in Engineering design in 2003 from Anna University Chennai, India, and Bachelor of Engineering in Mechanical Engineering in 1998 from Motilal Nehru National Institute of Technology Allahabad, India. Dr. Mishra started his academic career in 1998 after completing UG Mechanical Engineering at Kathmandu University, Dhulikhel, Nepal as a Lecturer. He received Brain Korea 21 (BK-21) scholarship by Government of Korea for his PhD study and Postdoctoral research at Ajou University, Suwon, South Korea. Dr. Mishra also worked as Asst. Professor at Ajou University. In his elven years of stay in South

Korea, he also worked as Senior Researcher at Advanced Institutes of Convergence Technology, Seoul National University, Suwon.

Dr. Nandakishor Yadav is working as a Scientist at the Fraunhofer Institute for Photonic and Microsystems. Before joining at IPMS, Germany, he served as a Senior Research Associate at Illinois Institute of Technology Chicago, USA. He also worked as a Post Doc fellow at the Indian Institute of Technology Indore. Dr. Yadav has completed Ph.D. in VLSI Design from the Indian Institute of Information Technology and Management Gwalior, India. His area of expertise is reliability SRAM cell, controller, peripheral circuit design, layout, DRC, PEX, and DFM. He has published number of peer reviewed articles, and demonstrated memory device technology to industry.