MANIPAL UNIVERSITY
JAIPUR

NAAC A+ Grade
with 3.28 Score

RANKINGS 2022
Engineering: 75
Management: 85
University:101-150

B.Tech.
Electronics Engineering (VLSI Design and Technology)

Design your own Degree and Career

Admission Booklet 2023-24

About the program

- Industry ready curriculum
- Various Research labs funded by industries
- Well established labs with upgraded tools
- MoU with renowned Universities and Industries
- Technical Clubs and Student Chapters
- Dedicated Mentorship
- Exposure to industries through industrial visits / interactions
- IAESTE student exchange program provides international
- Internship to the students
- Flexible scheme based on NEP

jaipur.manipal.edu
admissions@jaipur.manipal.edu

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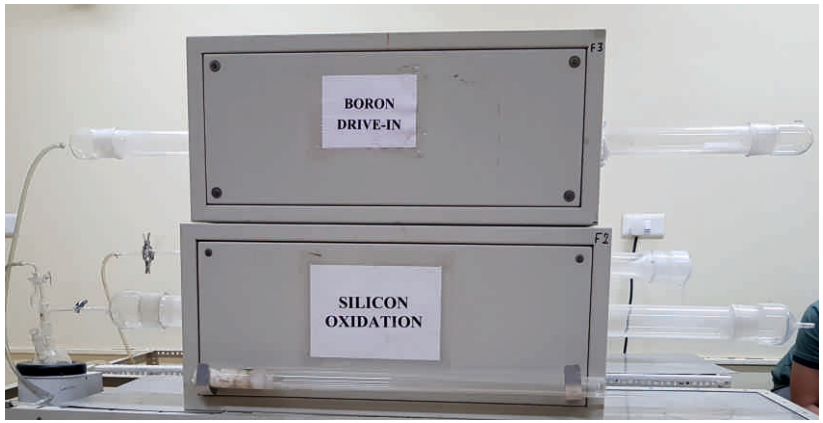
Key Highlights of the Program

- The India Semiconductor Mission (ISM) an initiative by Govt of India for growth of VLSI will help to have more placement opportunities in India
- The program is designed in line with the industry feedback and catering the needs of industry. It also includes the feedback of the stakeholders (Industry & Alumni)
- The program includes hands-on experience on EDA Tools
- Includes Industrial Internship
- Various technical student chapters and clubs
- Students can take their Major Project in VLSI Industries
- Association of VLSI Industry/Industries with this program
- Experienced & Skilled Faculty
- Advance Labs equipped with leading EDA tools
- Choice Based Credit System (CBCS)



Semi Conductor Fabrication Lab

Salient Feature of the Department

23 Teaching Staff	**100+** Abroad Higher Studies	**500+** Research Publications
900+ Alumni	**12** International & National MoU	**10** Student Club /Chapter

Internship/Placement opportunities in Industries

- Synopsys
- Mentor Graphics
- Cadence
- Microsoft
- Qualcomm
- Intel Technologies
- HCL Corporation
- einfochips
- Texas
- Synapse Design
- Infineon Technologies
- AMD Xilinx
- Samsung
- NXP Semiconductors
- ST Microelectronics
- Marvel Technologies

MoUs with Research Organizations and Industries

- Central Electronics Engineering Research Institute, Pilani
- Semi-conductor Laboratory, SAS Nagar
- Truechip Solutions, Noida
- Advanced Level Telecommunication Training Centre, Ghaziabad
- Secure Meters Ltd, Udaipur
- Samara National Research University
- University of Quebec
- University of KwaZulu-Natal, South Africa
- Swem Water Tech. (India) Pvt. Ltd., Jaipur
- Binus University, Indonesia
- University of Leicester, UK

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Unique Research And Lab Facilities

- Semiconductor Fabrication Lab
- FlexMEMS Research Center (FMRC)
- Optoelectronics and Photonics Research Lab
- VLSI & Embedded Lab

The MUJ EDGE (Why MUJ)

- NBA, NAAC A+, AICTE, and UGC Accredited Institution
- Academic excellence through world class curriculum, delivery & feedback
- Various scholarships for meritorious students offered by MUJ
- Excellent placements and internships
- Best-in-class academic, hostel and sport facilities
- Best-in-class infrastructure
- Qualified and Experienced faculty
- State-of-the-art Laboratories equipped with latest technology
- Student Travel Grant for International Internships
- Industry and International Collaborations

Eligibility

MET 2023 Rank Holders

The candidate must have passed 10+2 or A Level or IB or American 12th grade or equivalent examination from recognized board with Physics, Mathematics and English as Compulsory subjects, along with any one of Chemistry, Computer Science, Biotechnology, Biology, Statistics or Engineering Drawing as an optional subject for admission to B Tech, with minimum 50% marks in Physics, Mathematics and the optional subject, put together.

Direct admission is possible if seats are available after MET. Candidates need to meet one of the following criteria:

*Candidates have a JEE rank and qualified for JEE Advanced in that year

* Based on candidate's SAT score

* MET 2023 rank holders, who could not come for counseling.

* All Students with Physics, Mathematics and English as compulsory subjects and who have 50% or equivalent in PMX subjects in their 12th std. where X could be Chemistry, Computers Science, Biotechnology, Biology, Statistics or Engineering Drawing.

Core Competencies

- System Verilog Design and Verification
- Semiconductor Device Fabrication
- System on Chip (SoC)
- Application oriented Design (ASIC/FPGA)
- MOS VLSI Design
- Mixed Signal IC Design
- Physical Design
- IC Layout and Design
- Memory Design
- Computer Architecture and Processor Design
- Optical Sensors
- Micro-electromechnical Systems (MEMS)

Fee structure

Program	Program Fee (For 4 Years)	
	Indian (Rs)	International (USD)
BTech	13,23,000/-	28,300/-

More about the Department
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Research Areas

- Nanodevices & modelling
- Verification & Testing
- IC design & layout
- Low Power VLSI
- High Speed VLSI Design
- Mixed Signal IC Design
- MEMS devices
- Optical Sensors
- Memory Design

Career Opportunities

- ASIC frontend designer
- FPGA frontend designer
- ASIC physical design engineer
- AMS (Analog Mixed Signal) designer
- Library developer
- IP design engineer Verification Engineers
- Front-end verification engineer
- FPGA Back-end verification engineer
- Physical design verification engineer
- AMS verification engineer
- EDA tool validation engineer
- IP verification engineer
- Board validation engineer
- EDA/CAD Engineers

Key Student Achievements of Department

- Arunima Nauriyal, Summer Internship, University of Rochester, 2022
- Amogh Dyavangoudar, International Summer School, Karlshure School of optics and Photonics, 2022, USD 3000.
- MUJ Startup ALMIGHT* founded by Ashish Tummuri, B.Tech. ECE Batch (2019-2023), Mohit kumar Mishra B.Tech. ECE Batch (2019-2023) for securing "RUNNER UP" and PRIZE WORTH OF $10000 at KardiaChain Pioneer Program 2.0 international hackathon.
- Sonam Gour and Abha Sharma, Best paper Award, International Conference in Communication, Device and Networking (ICCDN-2022).
- Ashish Tummuri, Optics & Photonics Scholarship 2022, USD 3000
- Ashish Tummuri, SPIE for Photonics Europe Travel Grant,2022, USD 2000
- Tanvi Sharma, SPIE Officer Travel Grant 2020, USD 3000
- Rajdeep Mukherjee, SPIE Officer Travel Grant 2018, USD 3000
- Sayed Mujahid, IEEE Chapter Chair Meeting Grant 2018, USD 1500
- Aadhar Kapoor, SPIE Officer Travel Grant 2017, USD 3000
- Anshul Shrivastava, OSA Officer Travel Grant 2017, USD 3000

Scholarships

- TMA Pai Engineering Scholarships
- Scholarships for Lateral Entry (B. Tech.)
- TMA Pai Merit Scholarships
- Rajasthan Merit Scholarships
- Financial Assistance for Sibling(s)
- Scholarship for "Differently- abled" Students
- Scholarships for wards of Martyrs of Defence Personnel / Para
- Military Forces
- Scholarships for the wards of Single Mother & Orphan Child

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Department Alumni in VLSI Industries

ASIRBAD MISHRA
eInfochips Pvt Ltd

"The curriculum at MUJ developed my interest in VLSI beyond classroom and it helped me pursue a project in industry standard tools which later was published as a research paper due to the constant technical support and guidance from the college faculties. This blend of constant experimental learning as well as the classroom learning did help me crack the VLSI interviews that were conducted and gave me a foundation to pursue a career as a Physical Design Engineer at eInfochips Pvt Ltd (An Arrow Company)."

KARISHMA BABANI
Cadence

"My interest in VLSI domain was developed in Btech ECE undergrad program at Manipal University. The campus curriculum and courses offered provide a strong background for interviews at industry. Electronics faculty members educated us with laboratory sessions and shared there knowledgeable experiences in VLSI. The problem-solving and learner-centric environment has helped me attain required skills for projects, presentations and placements. Manipal University has provided me a perfect platform to shape my career in VLSI."

SATYAM
Synapse Design (Quest Global)

"The courses that were available in the curriculum for B.TECH like analog devices , linear integrated circuits, fundamentals of CMOS helped me get a good basic knowledge of how devices work it's circuit designing at BJT/MOS level and the semiconductor physics involved behind it. Moreover the program elective like Low power VLSI , developed an interest to further extend the gained knowledge beyond class room gave me a foundation to pursue a career as a Physical Design Engineer at Synapse Design (Quest Global)."

KARAN WADHWA
Cadence

"MUJ has given learning opportunities & helped me develop self belief with a positive relationship. It also introduced me to the digital world of VLSI(digital system design), associated lucrative career & bright future prospects.
Thanks to lot to MUJ and you for all the guidance and support"

ANUJ BHARDWAJ
ST Microelectronics

"The institute with its state of the art VLSI labs and faculty with great depth of knowledge made me pursue the VLSI field"

AISHANI
Synopsys

"MUJ was where I got introduced to VLSI, the world of semiconductors. It provides ample of opportunities to grow in your field of interest along with the guidance, constant support and encouragement from professors."

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Admission Process

Application form initiated through our website
admissions.jaipur.manipal.edu

Applicants must submit a completed application form with relevant documents within the due date.

Hostel Details

goodhostspaces.com **08069122800**
info.jaipur@goodhostspaces.com

Counsellor Contact Details

Ms Radhika
8306006860

For curriculum regarding please visit:

https://jaipur.manipal.edu/foe/programs/program-list/electronics-communication-engineering.html

Our counsellors will guide candidates through the admission process, which is as per regulatory requirements.

FAQ

Please visit the FAQ section on our website to know more about the admission process.

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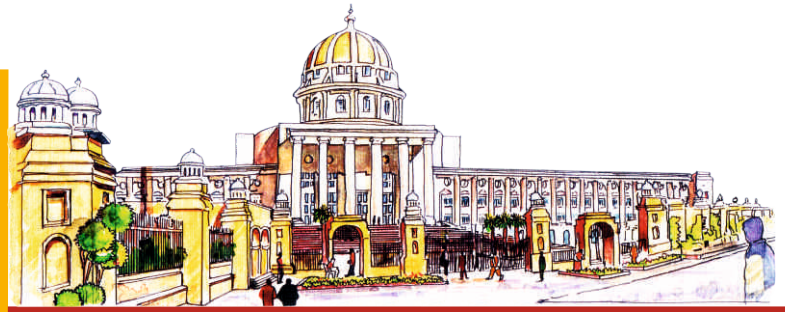

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(University Under Section 2(f) of the UGC Act)

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